**Open Ended Experiment**

**Digital Electronics and Computer Organization**

**(CSE 207)**

**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**



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**OPEN ENDED EXPERIMENT**

**AIM** - To stimulate 2-bit binary counter using circuit verse.

**TOOLS USED**- Circuit verse.

**THEORY-**

**Introduction of Sequential Circuits -**

A **Sequential circuit** combinational logic circuit that consists of inputs variable (X), logic gates (Computational circuit), and output variable (Z).

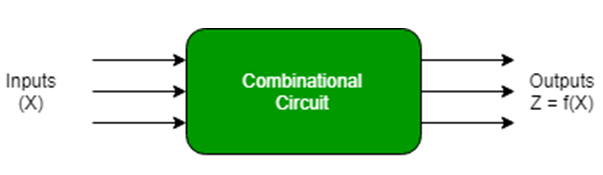


Fig 1: Combinational Circuit

Combinational circuit produces an output based on input variable only, but **Sequential circuit** produces an output based on **current input and previous input variables**. That means sequential circuits include memory elements which are capable of storing binary information. That binary information defines the state of the sequential circuit at that time. A latch capable of storing one bit of information.

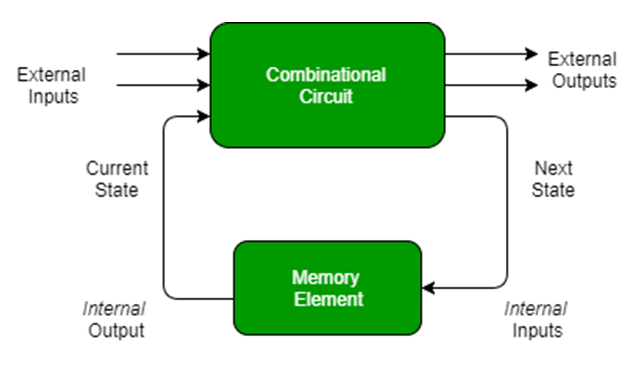


Fig 2: Sequential Circuit

As shown in figure there are two types of input to the combinational logic:

1. External inputs which not controlled by the circuit.
2. Internal inputs which are a function of a previous output states.

Secondary inputs are state variables produced by the storage elements, whereas secondary outputs are excitations for the storage elements.

**Types of Sequential Circuits –** There are two types of sequential circuit:

1. **Asynchronous sequential circuit –** These circuit **do not use a clock signal** but uses the pulses of the inputs. These circuits are **faster** than synchronous sequential circuits because there is clock pulse and change their state immediately when there is a change in the input signal. We use asynchronous sequential circuits when speed of operation is important and **independent** of internal clock pulse.

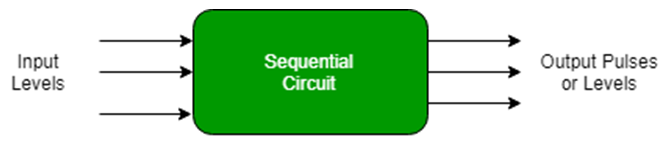


Fig 3: Asynchronous Sequential Circuit

But these circuits are more **difficult** to design and their output is **uncertain**.

1. **Synchronous sequential circuit –** These circuit **uses clock signal** and level inputs (or pulsed) (with restrictions on pulse width and circuit propagation). The output pulse is the same duration as the clock pulse for the clocked sequential circuits. Since they wait for the next clock pulse to arrive to perform the next operation, so these circuits are bit **slower** compared to asynchronous. Level output changes state at the start of an input pulse and remains in that until the next input or clock pulse.

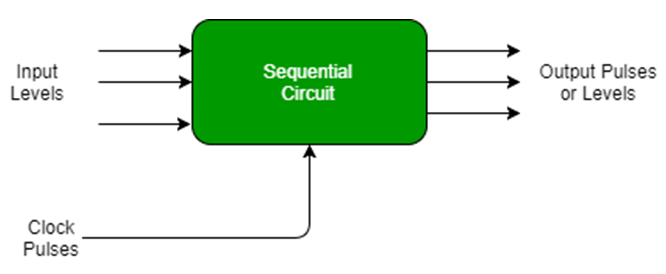


Fig 4: Synchronous Sequential Circuit

We use sequential circuits to design Counters, Registers, RAM, and other state retaining machines.

**Counters in Digital Logic -**

In digital logic and computing, a [**Counter**](https://en.wikipedia.org/wiki/Counter_(digital)) is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For example, in UP counter a counter increases count for every rising edge of clock. Not only counting, a counter can follow the certain sequence based on our design like any random sequence 0,1,3,2… .They can also  be designed with the help of flip flops.

**Counter Classification -**

Counters are broadly divided into two categories

1. Asynchronous counter
2. Synchronous counter

1. **Asynchronous Counter -** In asynchronous counter we don’t use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following flip flop is driven by output of previous flip flops. We can understand it by following diagram-

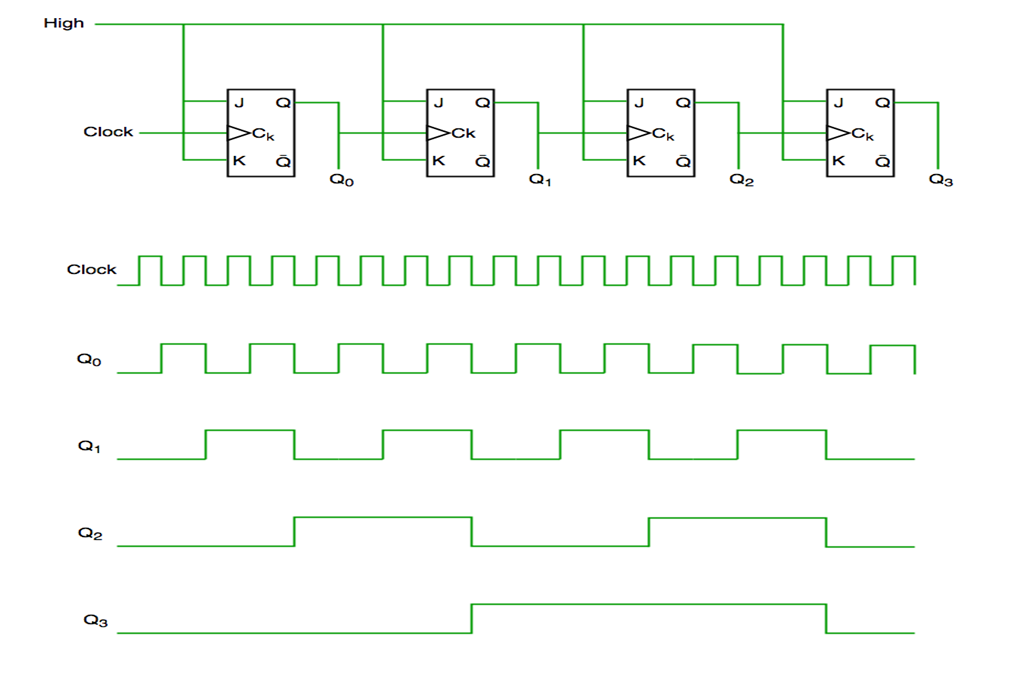
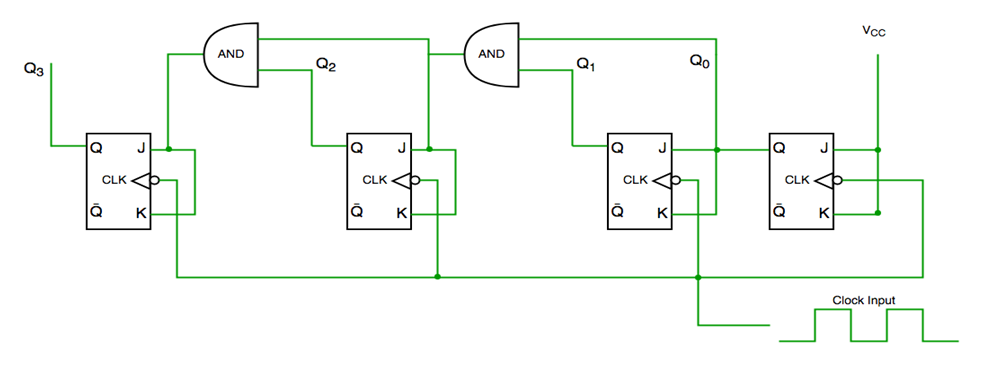


Fig 5: Asynchronous Counter Circuit and Its Timing Diagram

It is evident from timing diagram that Q0 is changing as soon as the rising edge of clock pulse is encountered, Q1 is changing when rising edge of Q0 is encountered(because Q0 is like clock pulse for second flip flop) and so on. In this way ripples are generated through Q0, Q1, Q2, Q3 hence it is also called **RIPPLE counter.**

2. **Synchronous Counter -** Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel. The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.



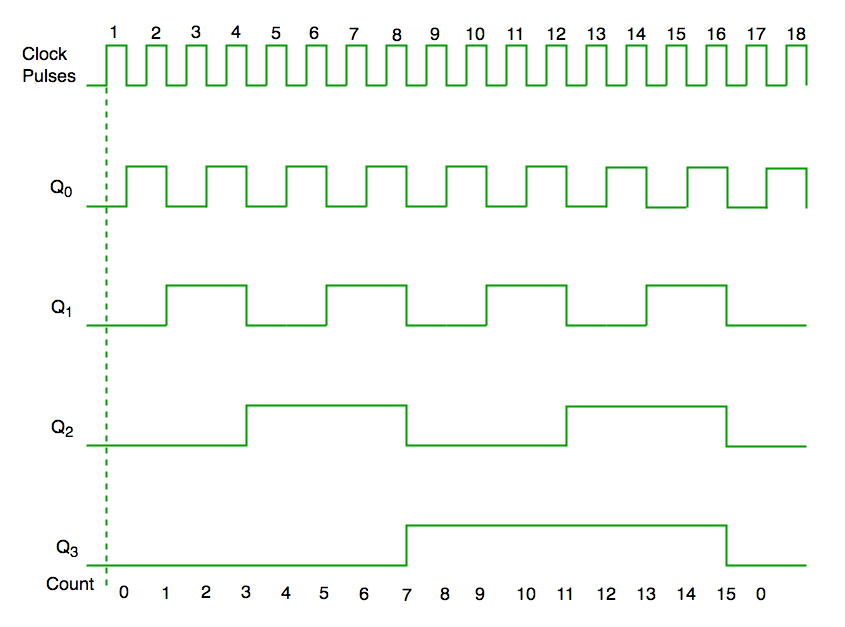


Fig 6: Synchronous Counter Circuit and Its Timing Diagram

From circuit diagram we see that Q0 bit gives response to each falling edge of clock while Q1 is dependent on Q0, Q2 is dependent on Q1 and Q0, Q3 is dependent on Q2,Q1 and Q0.

**JK FLIP FLOP -**

A JK flip flop is a refinement of the SR flip flop in that the indeterminate condition of the SR type is defined in the JK type. Inputs J and K behave like inputs S and R to set and clear the flip flop respectively. When inputs J and K are both equal to 1, a clock transition switches the outputs of the flip flop to their complement state. Instead of the indeterminate condition, the JK flip flop has a complement condition Q(t+1)=Q’(t) when both J and K are equal to 1.

|  |  |  |  |
| --- | --- | --- | --- |
| **J** | **K** | **Q(t+1)** |  |
| 0 | 0 | Q(t) | No change |
| 0 | 1 | 0 | Clear to 0 |
| 1 | 0 | 1 | Set to 1 |
| 1 | 1 | Q’(t) | Complement |

Table 1: Characteristic Table of JK Flip-Flop

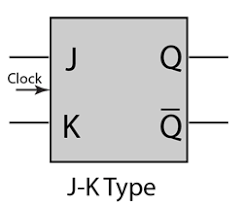


Fig 7: Graphical symbol of JK Flip-Flop

**EXCITATION TABLE -**

In [**electronics design**](https://en.wikipedia.org/wiki/Electronics_design), an **excitation table** shows the minimum inputs that are necessary to generate a particular next state (in other words, to **"excite"** it to the next state) when the current state is known. They are similar to [**truth tables**](https://en.wikipedia.org/wiki/Truth_table) and [**state tables**](https://en.wikipedia.org/wiki/State_table), but rearrange the data so that the current state and next state are next to each other on the left-hand side of the table, and the inputs needed to make that state change happen are shown on the right side of the table.

In order to obtain the excitation table of a [**flip-flop**](https://en.wikipedia.org/wiki/Flip-flop_(electronics)), one needs to draw the Q(t) and Q(t + 1) for all possible cases (e.g., 00, 01, 10, and 11), and then make the value of flip-flop such that on giving this value, one shall receive the input as Q(t + 1) as desired.

|  |  |  |  |
| --- | --- | --- | --- |
| **Q(t)** | **Q(t+1)** | **J** | **K** |
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

Table 2: Excitation Table of JK Flip-Flop

**BINARY COUNTER -**

A binary counter is basically a state machine that just cycles through its states for each cycle of a clock signal. A binary counter can be constructed from J-K flip-flops by taking the output of one cell to the clock input of the next. The J and K inputs of each flip-flop are set to 1 to produce a toggle at each cycle of the clock input. This produces a binary number equal to the number of cycles of the input clock signal. This device is sometimes called a "ripple through" counter. The same device is useful as a frequency divider.

**2 BIT BINARY COUNTER:**

A clocked sequential circuit that goes through a sequence of repeated binary states 00, 01, 10, and 11 when an external input x is equal to 1. The state of the circuit remains unchanged when, x = 0. This type of circuit is called a 2-bit binary counter because the state sequence is identical to the count sequence of two binary digits. Input x is the control variable that specifies when the count should proceed.

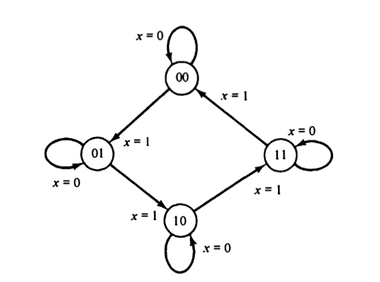


Fig 8: State Diagram of 2-Bit Binary Counter

The diagram is drawn to show that the states of the circuit follow the binary count as long as x = 1. The state following 11 is 00, which causes the count to be repeated. If x = 0, the state of the circuit remains unchanged. This sequential circuit has no external outputs, and therefore only the input value is labelled in the diagram. The state of the flip-flops is considered as **the outputs of the counter.**

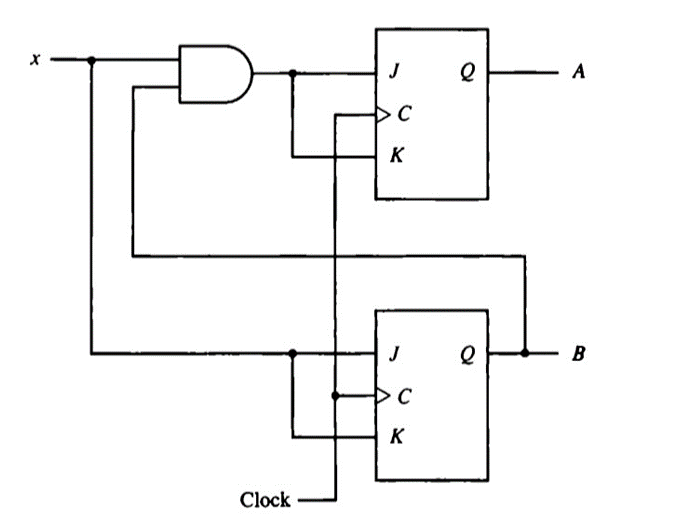


Fig 9: Circuit Diagram of 2-Bit Binary Counter

The symbol x is denoted to the input variable. Now, let us assign the symbols A and B to the two flip-flop outputs. The next state of A and B, as a function of the present state and input x, can be transferred from the state diagram into a state table. The first five columns of Table 3 constitute the state table. The entries for this table are obtained directly from the state diagram.

The excitation table of a sequential circuit is an extension of the state table. This extension consists of a list of flip-flop input excitations that will cause the required state transitions.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Present State** | | **Input** | **Next State** | | **Flip-Flop Input** | | | |
| **A** | **B** | **x** | **A** | **B** | **JA** | **KA** | **JB** | **KB** |
| 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | X |
| 0 | 0 | 1 | 0 | 1 | 0 | X | 1 | X |
| 0 | 1 | 0 | 0 | 1 | 0 | X | X | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | X | X | 1 |
| 1 | 0 | 0 | 1 | 0 | X | 0 | 0 | X |
| 1 | 0 | 1 | 1 | 1 | X | 0 | 1 | X |
| 1 | 1 | 0 | 1 | 1 | X | 0 | X | 0 |
| 1 | 1 | 1 | 0 | 0 | X | 1 | X | 1 |

Table 3: Excitation Table of 2-Bit Binary Counter

The truth table for the combinational circuit part of the sequential circuit is available in the excitation table. The present-state and input columns constitute the inputs in the truth table.The flip-flop input conditions constitute the outputs in the truth table.

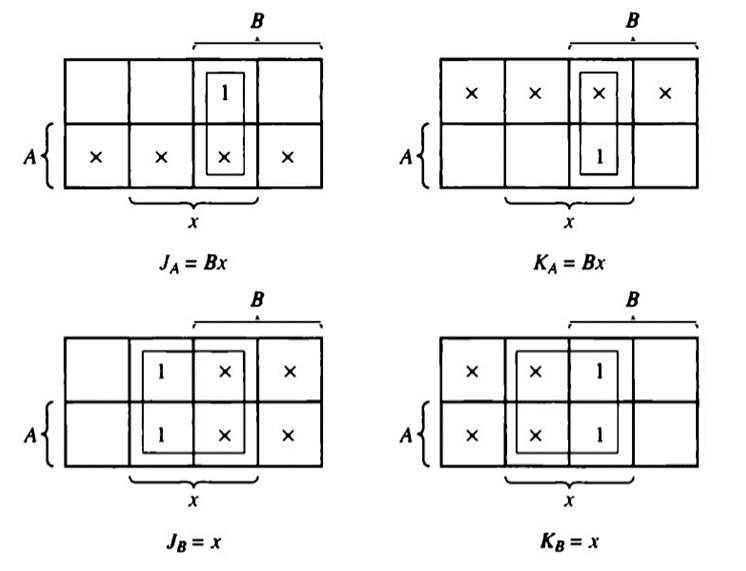
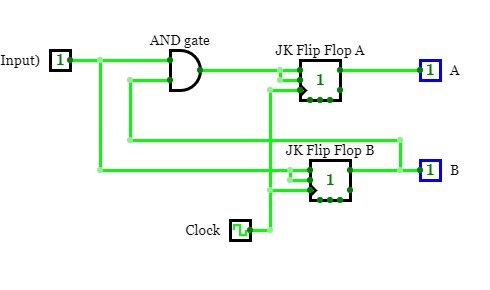


Fig 10: K-map Representation of JK Flip-Flop

**OBSERVATIONS –**

Circuit diagram of 2-Bit Binary Counter drawn with the help of Circuit Verse:



**CONCLUSION:**

A **Sequential circuit** combinational logic circuit that consists of inputs variable (X), logic gates (Computational circuit), and output variable (Z). **Sequential circuit** produces an output based on **current input and previous input variables**.

A JK flip flop is a refinement of the SR flip flop in that the indeterminate condition of the SR type is defined in the JK type. Inputs J and K behave like inputs S and R to set and clear the flip flop respectively. When inputs J and K are both equal to 1, a clock transition switches the outputs of the flip flop to their complement state.

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